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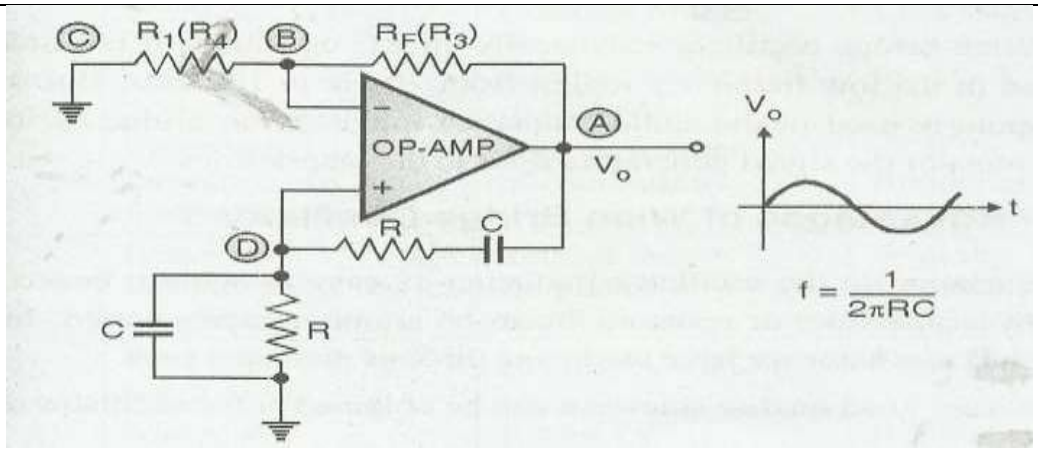
WINTER – 19EXAMINATION

Subject Name: Linear Integrated Circuit **Model Answer** Subject Code: 22423

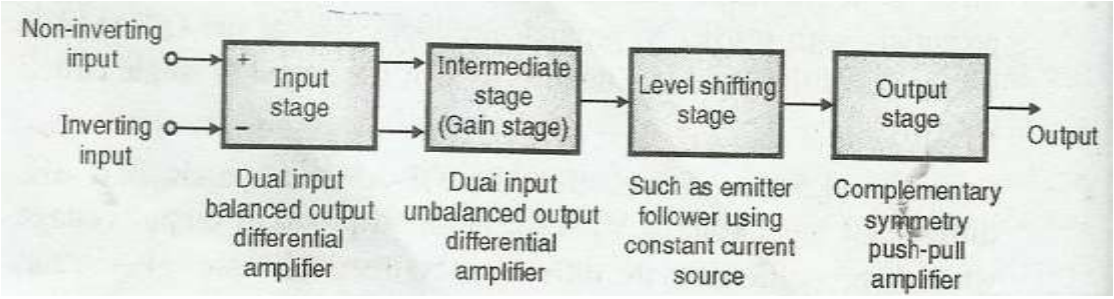
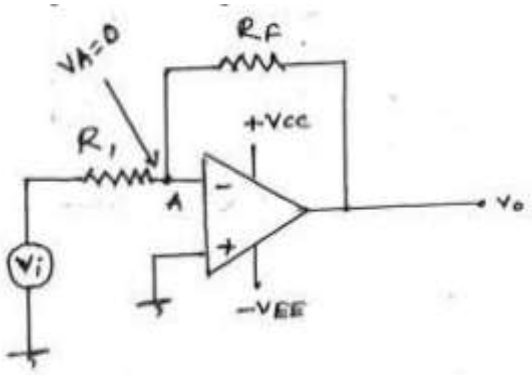
Important Instructions to examiners:

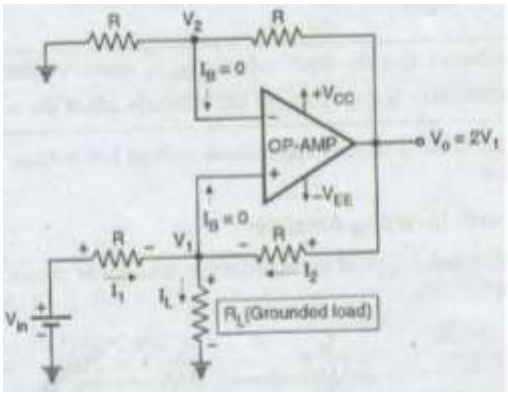
1) The answers should be examined by key words and not as word-to-word as given in themodel answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may tryto assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given moreImportance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in thefigure. The figures drawn by candidate and model answer may vary. The examiner may give credit for anyequivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constantvalues may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

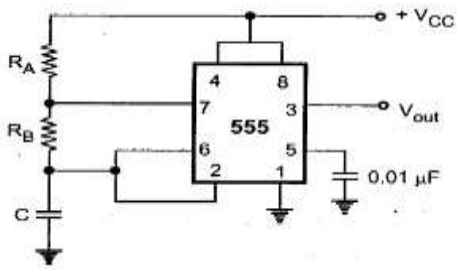
Q. No.	Sub Q. N.	Answer	Marking Scheme
Q.1		**Attempt any FIVE of the following:**	**10-Total Marks**
	a)	**Define the operational amplifier parameters.** **i)Slew rate** **ii) Input bias current**	**2M**
	Ans:	i) Slew Rate: it is defined as the maximum rate of change of o/p voltage per unit time & its 0.5 per volt/use [S.R=∞]. ii) Input Bias Current: Input Bias Current is the average of the currents entering into the positive & negative terminals of an op-Amp & its value is 200 nA	**1M Each**
	b)	**Draw Wien bridge oscillator circuit using IC 741.**	**2M**
	Ans:		**2M**
	c)	**List four specifications of IC LM324.**	**2M**

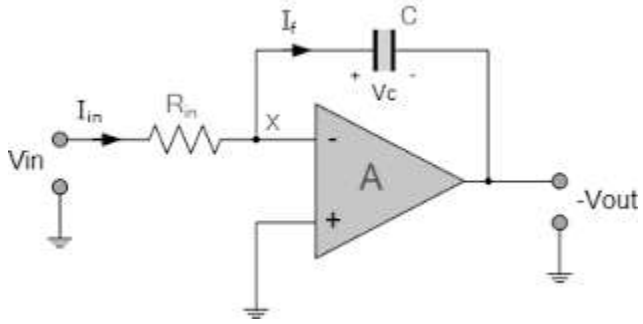
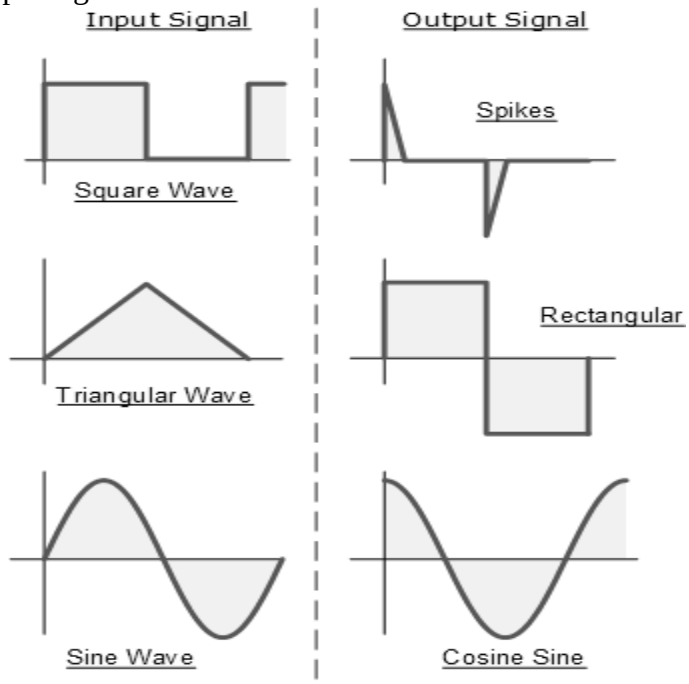
	Ans:	1. Integrated with four Op-Amps in a single package 2. Wide power supply Range i) Singe supply – 3V to 32V ii) Dual supply – ±1.5V to ±16V 3. Low Supply current – 700uA 4. Single supply for four op-amp operation enables reliable operation 5. Operating ambient temperature – 0˚C to 70˚C 6. Soldering pin temperature – 260 ˚C (for 10 seconds – prescribed)	**½ M Each**
	d)	**State the four applications of an instrumentation amplifier.**	**2M**
	Ans:	The instrumentation amplifier can be used for other application such as 1. Electronic weighing machine scale 2 .Light, intensity meter 3. Pressure monitoring & controlling 4. Temperature monitoring and controlling. 5. Process Instrumentation in measurement of physical quantities.	**½ M Each**
	e)	**State the four advantages of active filter over passive filter.**	**2M**
	Ans:	Advantages of active filter over passive filter: 1. Gain and frequency adjustment flexibility since the op-amp is able to providing gain; the input signal is not attenuated as in case of passive filters. 2. Active filter is easier to tune or adjust as compare to passive filters. 3. No loading problem because active filter provides excellent isolation between individual stages due to high input impedance. 4. Active filters are small in size and less bulky (due to absence of "L") and rugged. 5. Non floating input and output.	**½ M Each**
	f)	**Define roll of rate and order of filter.**	**2M**
	Ans:	1. Roll of rate is the rate of change of gain with frequency. Roll of rate is always measured in dB/decade. 2. The roll of rate is called the order of the filter. It depends on the rate at which filter's gain changes with frequency. For example: i) If roll off rate is -20 dB / decade or +20 dB / decade then the filter is of 1st order. ii) If roll of rate is-40 dB / decade or +40 db / decade then the filter is of 2nd order and so on	**2M**
	g)	**State the function of following pins of IC 555** **i) Threshhold** **ii) Discharge**	**2M**
	Ans:	i) Threshhold voltage- When positive going pulse is applied at this pin but it is more positive than reference voltage (2/3vce) of upper comparator. Hence, o/p of upper comparator becomes high i.e. S=0, R=1. Due to this, flip-flop becomes reset that's why $\bar{Q}$=1 which goes to base of NPN transistor is ON & the external capacitor ct starts discharging to transistor to words zero. At the same time, the o/p of timer goes low. ii) Discharge- The external capacitor Ct is connected at this pin and capacitor discharge through this pin	**2M**

Q.2		**Attempt any THREE of the following:**	**12-Total Marks**

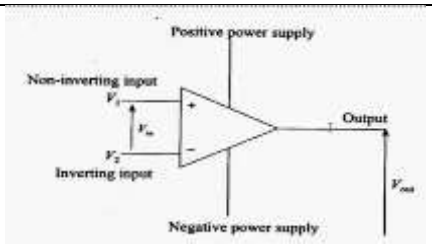
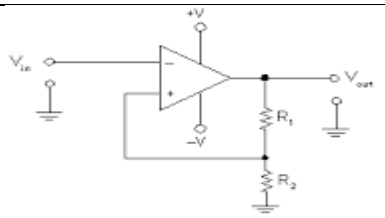
	a)	**Describe the block diagram of op-amp.**	**4M**
	Ans:	**Block Diagram:**  The OP-AMP is basically a different amplifier i.e. it will amplify the voltage which is differentially present between its input terminals. 1. Input stage: The input stage is a dual-input, balanced output differential. The two inputs are inverting and non-inverting input terminals. This stage provides most of the voltage gain of the OP-AMP and decides the input resistance value R_1. 2. Intermediate stage: This is usually another differential amplifier. It is driven by the output of the input stage. This stage is a dual-input unbalanced output (single ended output) differential amplifier. 3. Level shifting stage: Due to the direct coupling between the first two stages, the input of level shifting stage is an amplified signal with some non-zero dc level. Level shifting stage is used to bring this dc level to zero volts with respect to ground. 4. Output stage: this stage is normally a complementary output stage. It increases the OP-AMP. It also provides a low output resistance.	**1M** **3M Explanation**
	b)	**Explain with neat circuit diagram, the significance of virtual ground in an op-amp.**	**4M**
	Ans:	Virtual ground concept:-In circuit point A is virtual ground. Figure shows inverting amplifier using op-amp. In this circuit non-inverting terminal is connected to the actual ground. Due to this potential of inverting terminal become zero. Thus, inverting terminal is not actually connected to the ground. There after its potential is zero. Thus point A is known as virtual ground point. This phenomenon of having zero potential without actually grounding is known as virtual ground concept. **Circuit diagram:** 	**3M Explanation** **1M**

	c)	**Draw the circuit diagram of grounded load type V to I converter and derive expression for its output.**	**4M**
	Ans:	**Diagram:** 	**2M**
		• The analysis of the circuit can be done by following two steps: First step is to determine the voltage V_1 at the non- inverting (+) terminal and the second step is to establish relationship between V_1 and the load current I_L. • Applying KCL at node V_1, $I_1 = I_1 + I_2$ ---------- (1) But $I_1 = V_{in} - V_1 / R$ and $I_2 = V_o - V_1 / R$, Substituting these expression into equation (1) $$I_L = \frac{V_{in} - V_1}{R} + \frac{V_o - V_1}{R}$$ $$\therefore \quad V_{in} + V_o - 2V_1 = I_L R$$ $$\therefore \quad V_1 = \frac{V_{in} + V_o - I_L R}{2} \quad \text{-----(2)}$$ as we have obtained the expression for V1.	**2M**

		• The OP- AMP is connected in the non- inverting mode. Therefore gain of the circuit is, $A_{VF} = 1 + \frac{R}{R} = 2.$ • The output voltage is given by, $V_o = A_{VF} \times V_1 = 2V_1$ • Substituting V1 from equation (2) we get, $V_o = V_{in} + V_o - I_L R$ $\therefore I_L R = V_{in}$ $\therefore I_L = \frac{V_{in}}{R}$ ----(3)	
	d)	**Sketch the astable multivibrator using IC 555 and explain it.**	**4M**
	Ans:	**Circuit:**  When the flip-flop is set, Q is high which drives the transistor Qd in saturation and the capacitor gets discharged. Now the capacitor voltage is nothing but the trigger voltage. So while discharging, when it becomes less than 1/3 V_{cc}, comparator 2 output goes high. This resets the flip-flop hence Q goes low and Q goes high. The low Q makes the transistor off. Thus capacitor starts charging through the resistances R_A, $R_B$and V_{cc}. As total resistance in the charging path is (R_A + R_B), the charging time constant is (R_A + R_B) C. Now the capacitor voltage is also a threshold voltage. While charging, capacitor voltage increases i.e. the threshold voltage increases. When it exceeds 2/3 V_{cc}, then the comparator 1 output goes high which sets the flip-flop. The flip-flop output Q becomes high and output at pin 3 i.e. Q becomes low. High Q drives transistor Q_d in saturation and capacitor starts discharging through resistance R_8 and transistor Q_d. Thus the discharging time constant is R_B C. When capacitor voltage becomes less than 1/3 V_{cc}, comparator 2 output goes high, resetting the flip-flop. This cycle repeats. Thus. when capacitor is charging, output is high while when it is discharging the output is low. The output is a rectangular wave. The capacitor voltage is exponentially rising and falling.	**2M** **2M Explanation**
Q.3		**Attempt any THREE of the following:**	**12-Total Marks**

	a)	**Describe the basic integrator circuit using op-amp.**	**4M**
	Ans:	The basic operational amplifier integrator circuit consists of an op amp with a capacitor between the output and the inverting input, and a resistor from the inverting input to the overall circuit input as shown in figure.  Equation for output of integrator as shown below where input is Vin and Rin input resistance and C is capacitor $V_{out} = -\frac{1}{R_{in}C}\int_0^t V_{in}\,dt = -\int_0^t V_{in}\frac{dt}{R_{in}.C}$ By equation it is understood that output is proportional integration of input voltage. Output of given input signal as shown below.  	**2M explanation with equation** **1M for Diagram** **1M for any one output waveform**
	b)	**Compare comparator and Schmitt trigger circuit (any four points).**	**4M**
	Ans:		**1M each any 4 point**

Sr. No	Parameter	Comparator	Schmitt Trigger
1	Feedback	Absent i.e. open loop	Present i.e. closed loop
2	Hysteresis	Absent	Present

3	Number of reference	One	TWO (UTP and LTP)	
4	Application	Zero crossing detector, Level detector	Sine wave to Square wave generator, pulse counter	
5	Definition	Comparator compare two signal one is called reference and other is called input signal	Schmitt trigger is inverting comparator with positive feedback	
6	Noise Margin	Low	More	
7	Level	single	Double	
8	Diagram			

c) **Design a first order low pass filter at a cut off frequency 12KHz with pass band gain '2'(assume C=0.01μF)** **4M**

Ans:

F_h = 12Khz ,A_f=2

A_f=1 + R_f/ R_1

2= 1 + R_f/ R_1

R_2/ R_1 =1

Assume R_f=10K = R_1

Fh= 1/2πRC

12K=1/2πRC

R=1/2πX 12KX.01μF

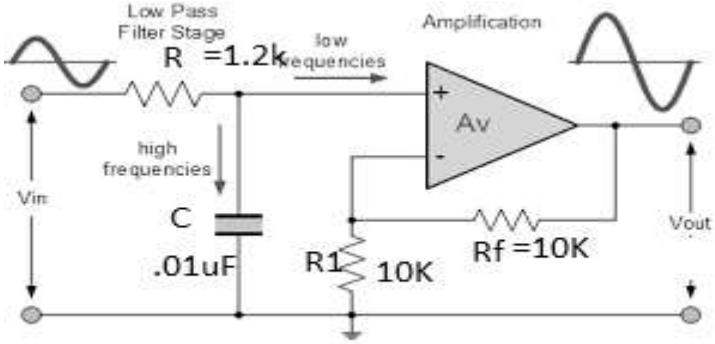
R=1.326 KΩ Actual value (1.2 KΩ)

2 M Resistor for feedback

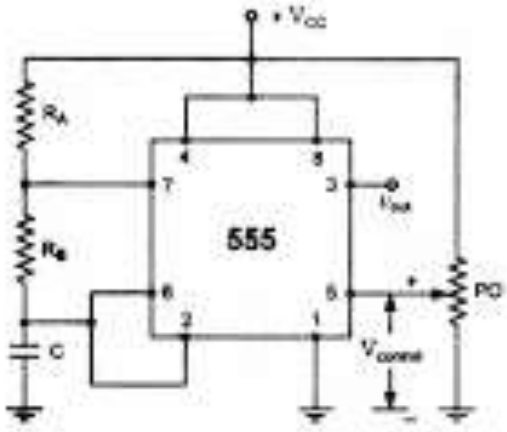
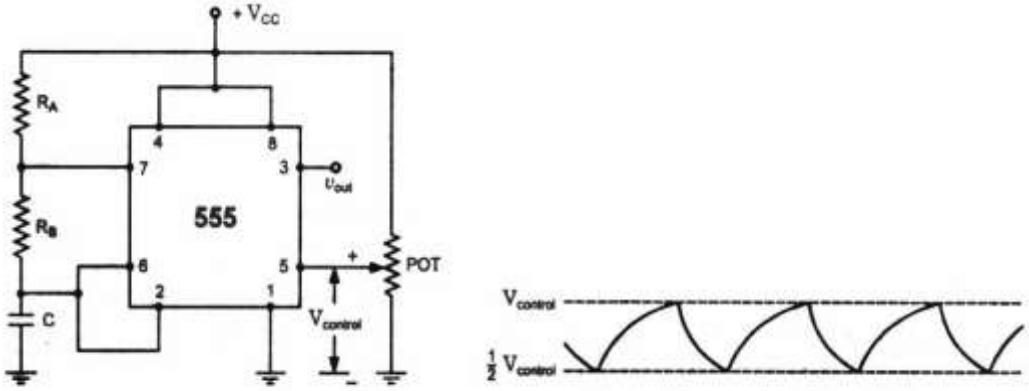
(1M for formula)

2M for Resistor of cut off frequency (1 for formula)

Circuit Diagram:



d) **Explain the working of IC 555 as a voltage controlled oscillator(VCO)** **4M**

	Ans:	**Diagram: -**  Circuit A voltage controlled oscillator is an oscillator whose frequency is controlled by an input voltage. Basically, the voltage input into the VCO controls how many times a digital signal will oscillate in a given time period. It is basically astable multivibrator configuration in which pin 5 is connected to variable voltage terminal in which square wave generator which output frequency can vary by varying voltage at pin 5. **OR**  Circuit Timing Capacitor Voltage Waveform *Voltage Controlled Oscillator* Pin 5 terminal is voltage control terminal and its function is to control the threshold and trigger levels. Normally, the control voltage is ++2/3V_{CC} because of the internal voltage divider. However, an external voltage can be applied to this terminal directly or through a pot, as illustrated in figure, and by adjusting the pot, control voltage can be varied. Voltage across the timing capacitor is depicted in figure, which varies between +$V_{control}$ and ½ $V_{control}$. If control voltage is increased, the capacitor takes a longer to charge and discharge; the frequency, therefore, decreases. Thus the fre-quency can be changed by changing the control volt-age.	**2M diagram** **2M explanation**
Q.4		**Attempt any THREE of the following :**	**12-Total Marks**
	a)	**Compare open loop and closed loop configuration of operational**	**4M**

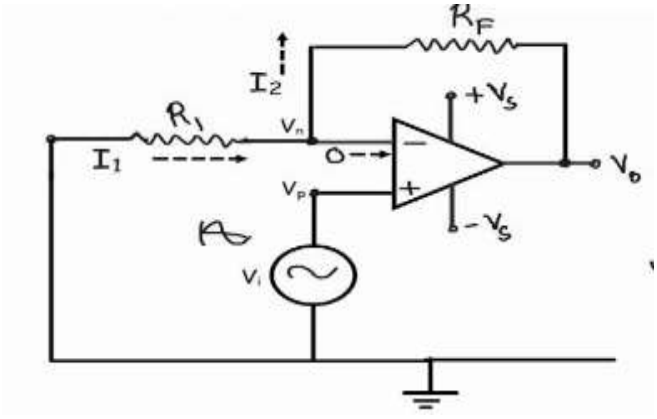
amplifier(any four points)

Ans: **4M**

Sr. No	Parameter	Open Loop Configuration	Closed loop configuration
1	Feedback	Absent	Present
2	Voltage Gain	High ideally infinite	Low
3	Gain control	Not possible	possible
4	Input Resistance	No change or Cannot Control	Can Control by adjusting feedback component
5	Output Resistance	No change or Cannot Control	Can Control by adjusting feedback component
6	Bandwidth	No change or Cannot Control	Can Control by adjusting feedback component
7	Offset voltage	No change or Cannot Control	Can Control by adjusting feedback component
8	Application	Comparator	All application circuit such as amplifier, oscillator, filter ,adder subtract or and so on
9	Stability	unstable	stable

b) **Sketch the circuit diagram of closed loop non-inverting amplifier and derive expression for its gain.** **4M**

Ans: **Diagram:** **2 M**



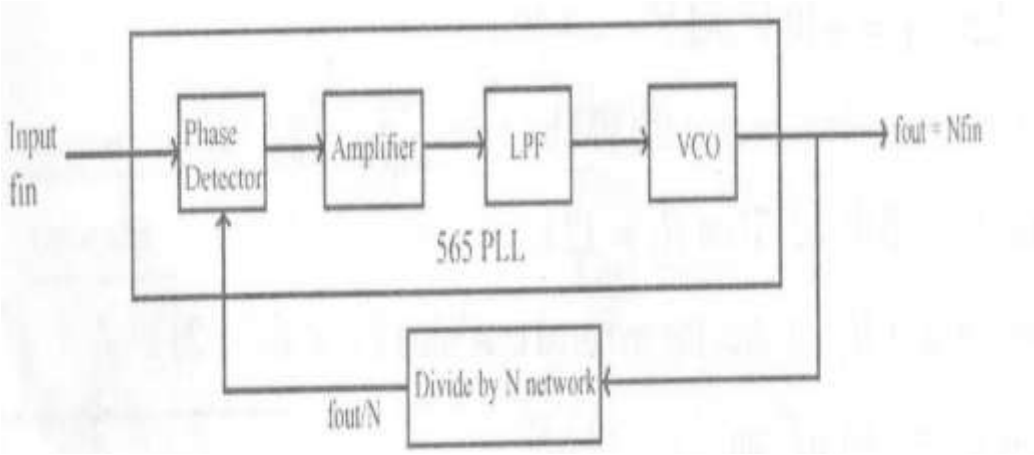
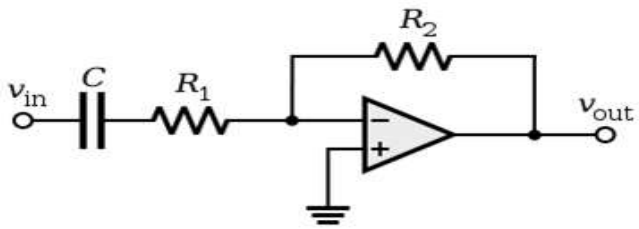
As per virtual ground concept $V_n = V_p = Vi$

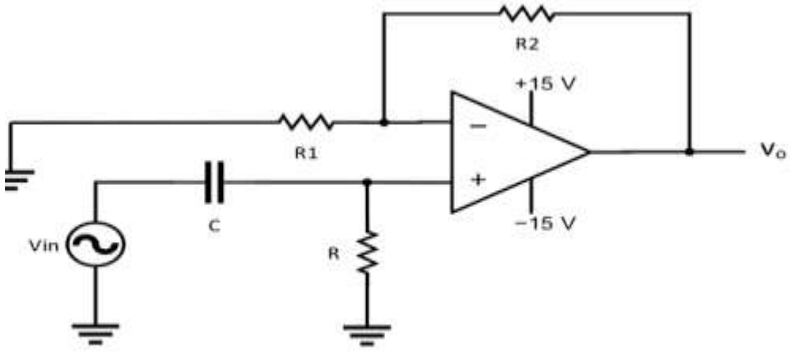
Where Vn is node voltage at inverting terminal and Vi is input voltage

$Vn=Vi=R_1 \times I_1$

$Vo= Rf \times I_2 + R_1 \times I_1$

2M Explanation

		Since no current is flow between inverting and non inverting terminal $I_1=I_2=I$ Vi=R1X I Vo=Rf X I + R_1XI Voltage Gain= Vo/ Vi = (Rf X I + R_1XI)/ R1X I =(Rf +R1)/R1 = 1+Rf/R1	
	c)	**Explain the working of PLL as multiplier using block diagram.**	**4M**
	Ans:	**Diagram:-**  A frequency multiplier can be designed using a PLL and a 'divided by N' counter. The frequency divider is inserted between the VCO and phase detector of PLL circuit. Therefore, one input of the phase comparator is the input signal and the other is the output of 'divided by N' counter. when the lock is established the input frequency fin equals the output of the counter fn. hence fin=fn= (fout)/N where foutis the VCO output frequency, Therefore, fout =NX fin. Thus when the system is in lock, the VCO is actually running at the multiple of input frequency. The desired amount of multiplication can be obtained by selecting a proper divide by N network, where N is an integer.	**2M** **2M**
	d)	**Draw the neat circuit diagram of first order high pass filter and explain its operation.**	**4M**
	Ans:	**Diagram:-** **Inverting filter**  **OR**	**2M**



$$G = 1 + \frac{R_2}{R_1}$$

$$f_c = \frac{1}{2\pi RC}$$

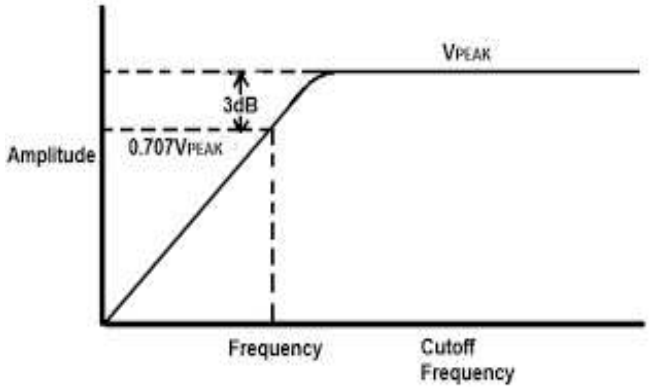
Non Inverting Filter

Active high pass filter is the filter network with OP-Amp as active element. The High Pass filter filter is one whose output above cut off is constant and same as input or higher depending on the gain of amplifier.

For first order filter the Roll off rate 20 db per decay It consist of RC network at input and with feedback resistor for increase gain filter network can be connected at noninverting terminal where resistive network at inverting loop for gain control.

Equation for cutoff frequency

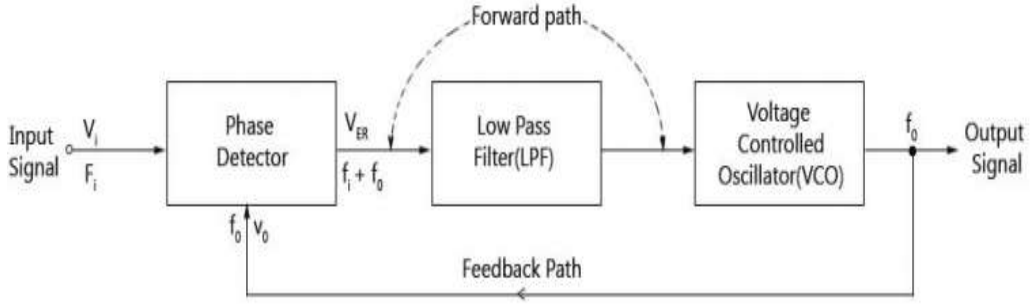
Fc=1/2πR1C



Graph

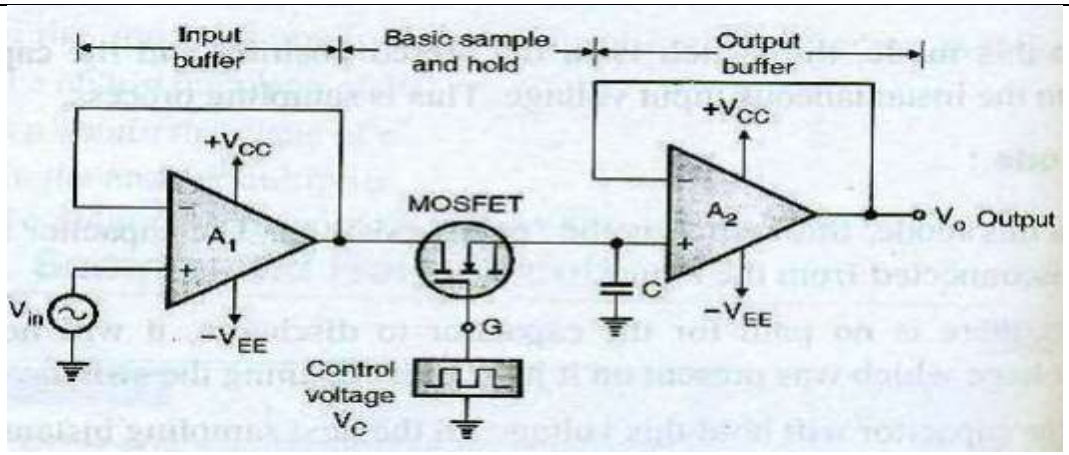
2 M for explanation with graph

	e)	**Explain the block diagram of phase locked loop.**	**4M**
	Ans:	**Diagram:**	**2M**

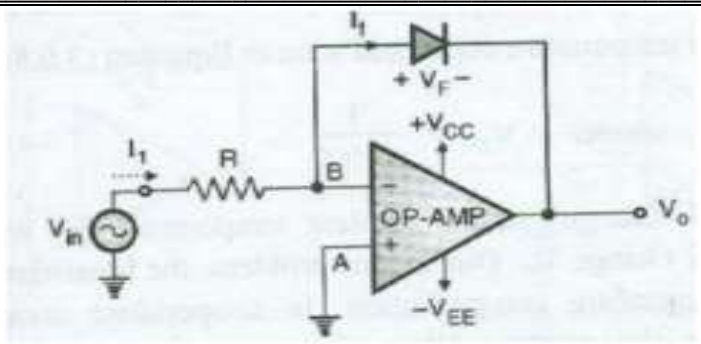


PLL is Phase locked loop is basic closed loop system used for different frequency and phase control application. It consists of Phase detector, Low Pass filter and Voltage controlled oscillator circuits.

2M

		Phase Detector: The input signal 'Vi' with an input frequency 'Fi' is conceded by a phase detector. Basically the phase detector is a comparator that compares the input frequency fi through the feedback frequency fo. The output of the phase detector is (fi+fo) which is a DC voltage. **Low Pass Filter:** The out of the phase detector, i.e., DC voltage is input to the low pass filter (LPF); it removes the high-frequency noise and produces a steady DC level, i.e., Fi-Fo. The Vf is also a dynamic characteristic of the PLL **VCO:** The output of the low pass filter, i.e., DC level is passed on to the VCO. The input signal is directly proportional to the output frequency of the VCO (fo). The input and output frequencies are compared and adjusted through the feedback loop until the output frequency is equal to the input frequency. Hence, the PLL works like free running, capture, and phase lock.	
Q.5		**Attempt any TWO of the following**	**12 Total Marks**
	(a)	**Explain the function of sample and hold circuit by using op-amp.**	**6M**
	Ans:	 The n-channel MOSFET is driven by a control voltage VC acts as a switch. The control voltage VC is applied to the gate of the MOSFET. The circuit diagram can be split into three stages. First stage is the voltage follower second one is the switch and capacitor and the third one is a gain the voltage follower. When VC is high the MOSFET turns on and acts like a closed switch .This is sampling mode .The capacitor charges through the MOSFET to the instantaneous input voltage. As soon as VC=0 the MOSFET turns off and the capacitor is disconnected from OPMP1 output. Capacitor cannot discharge through amplifier A2 due to its high impedance. Thus this is the hold mode in which the capacitor holds the latest sample value. The time period during which the voltage across capacitor is equal to input voltage is called sample period. The time period during which the voltage across capacitor is constant is called Hold period.	**Circuit diagram-3M** **Explanation - 3M**
	(b)	**Explain the circuit diagram of logarithmic amplifier using op-amp.**	**6M**

Ans:



The expression for the current passing through diode is always given by,

$$I_F = I_O\left(e^{\frac{V_F}{V_T \eta}} - 1\right)$$

Where,

$$I_F = Feedbackcurrentthroughdiode$$

$$I_O = Reversesaturationcurrent$$

$$V_F = Forwardvoltagedrop$$

Ƞ = constant i.e. 1 for Ge& 2 for Si

$$V_T = \frac{KT}{q}$$

K = Boltzmann's constant = $1.38 * 10^{-23}$

T = Temperature in Kelvin [$273K = 0°C$]

q = Electric charge = $1.692* 10^{-19}$ C

As $e^{\frac{V_F}{V_T \eta}} \gg 1$

$$\therefore I_F = I_O\left(e^{\frac{V_F}{V_T \eta}}\right)$$

$$\frac{I_F}{I_O} = \left(e^{\frac{V_F}{V_T \eta}}\right)$$

Taking natural log on both side,

$$log_e\left(e^{\frac{V_F}{V_T \eta}}\right) = log_e\left(\frac{I_F}{I_O}\right)$$

$$\frac{V_F}{\eta V_T} log_e e = log_e\left(\frac{I_F}{I_O}\right)$$

As $log_e e = 1$

$$\therefore \frac{V_F}{\eta V_T} = log_e\left(\frac{I_F}{I_O}\right)$$

$V_F = \eta V_T log_e\left(\frac{I_F}{I_O}\right)$ ..... (1)

Now from figure,

$$V_F = V_B - V_O$$

$V_F = -V_O$ (Since $V_B = 0\ from virtual ground concept$)

$$-V_F = V_O$$

$\therefore V_O = -\eta V_T log_e\left(\frac{I_F}{I_O}\right)$ ..... (2)

Now apply KCL at node B,

$$I_1 = I_B + I_F$$

$$\therefore I_1 = I_F$$

$$\therefore \frac{V_i - V_B}{R_i} = I_F$$

$\therefore I_F = \frac{V_i}{R_i}$ (Since $V_B = 0\ from virtual ground concept$)

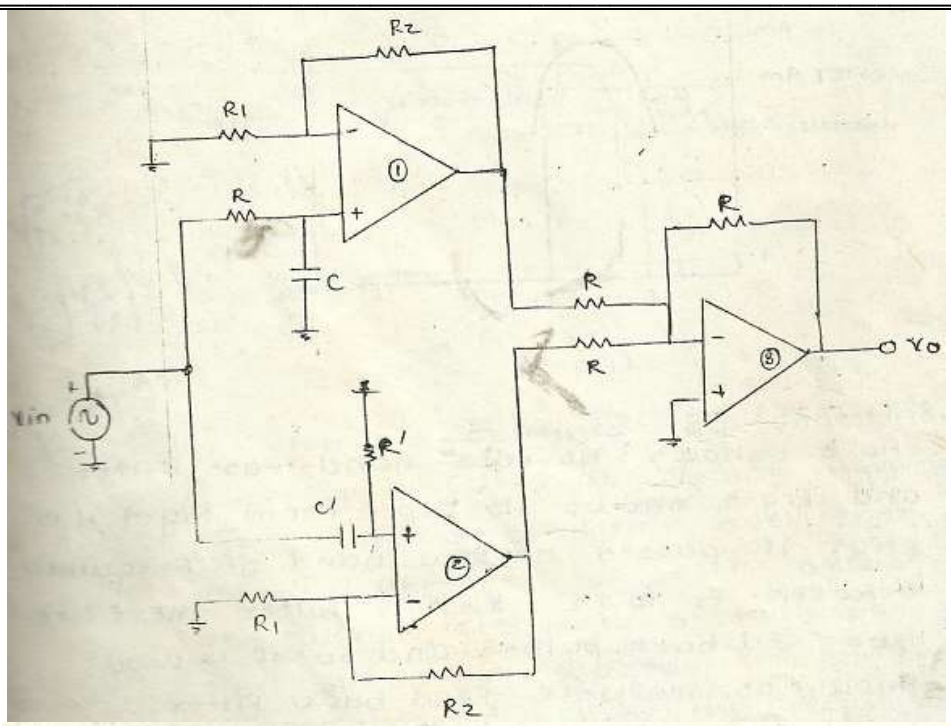
Put this into eqn 2

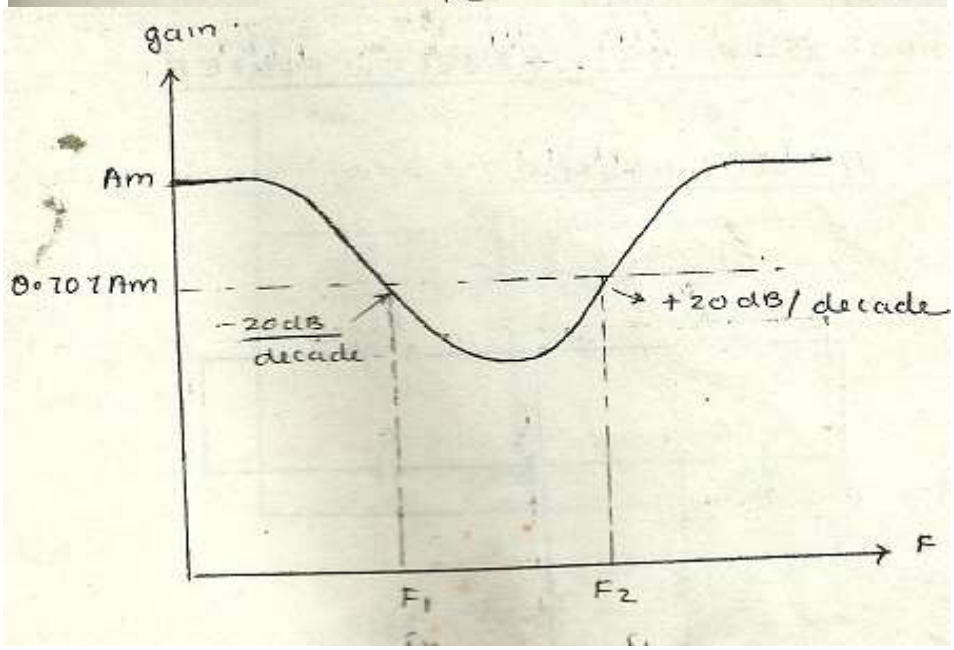
$$V_O = -\eta V_T log_e\left(\frac{V_i}{R_i I_O}\right)$$

$\therefore V_O \propto log_e V_i$

	(c)	**Sketch the circuit diagram of active wide band reject filter and explain it.**	**6M**

Ans:



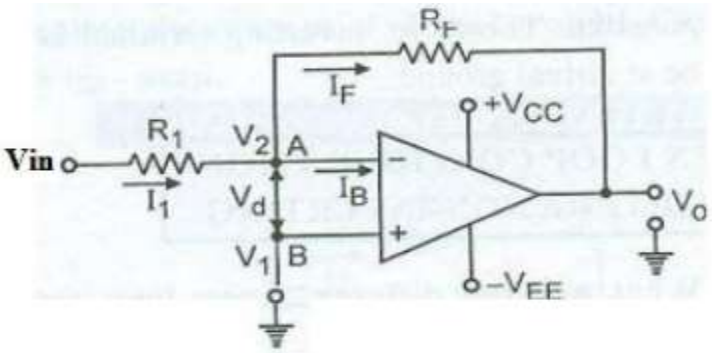


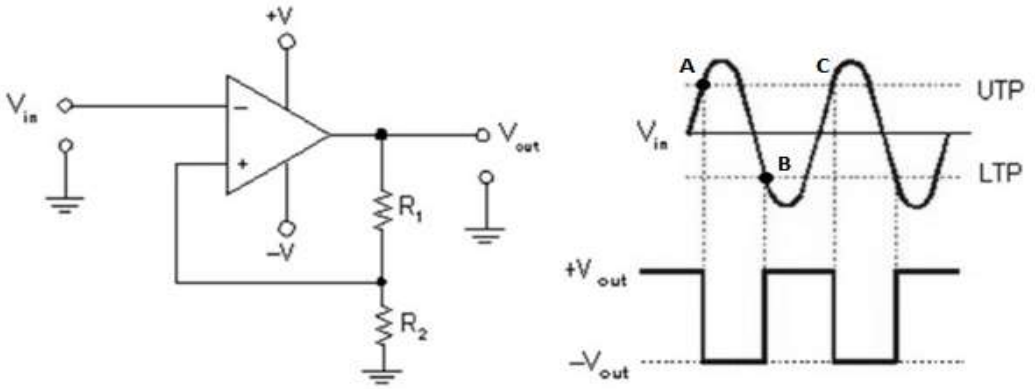
This filter is obtained by applying input simultaneously to low pass filter and high pass filter o/p of both the filters are given to adder CKT. Here we have designed that the cut off frequency of LPF must be less than cut off frequency of high pass filter.

Figure-1 shows CKT diagram of BRF and figure -2 shows corresponding o/p op-amp

1. Acts like LPF & op-amp
2. Acts like HPF . op-amp
3. Acts like adder ckt grom frg-2 it $_1$3 clear that this ckt passes all the frequencies except the frequencies between F_1 & Fz.

Q.6		**Attempt any TWO of the following:**	**12 Total Marks**

	(a)	**Sketch the circuit diagram of closed loop inverting amplifier and obtain output expression.**	**6M**
	Ans:	Inverting Amplifier using Op-Amp: **Circuit Diagram:**  Derivation for gain: Apply KCL at node A, we get $$I_1 = I_F + I_B \quad ----(1)$$ But ideally Input impedance of op amp is infinite, Therefore $$I_B = 0$$ $$I_1 \cong I_F$$ $$\frac{Vin - V2}{R1} = \frac{V2 - Vo}{RF}$$ According to virtual ground condition, $$V1 = V2 = 0$$ $$\frac{Vin}{R1} = \frac{-Vo}{RF}$$ $$V_o = -\left(\frac{R_F}{R_1}\right) V_{in} \quad ------(2)$$ $$A_V = \frac{Vo}{Vin} = -\left(\frac{R_F}{R_1}\right) \quad ------(3)$$ Where, Av is closed voltage gain	**Diagram-3M** **Derivation of output expression-3M**
	(b)	**Explain Schmitt trigger circuit using Op-amp and how UTP and LTP are calculated.**	**6M**
	Ans:	**Diagram:**	**2M**



A Schmitt trigger converts an irregular shaped waveform into a square wave. It uses positive feedback. It is a special type of comparator in which the output changes from one saturation level to other depending on differential input voltage.
Before applying any input, the output is assumed to be small and positive. This is the output offset voltage. The differential voltage Vid is positive; hence the output is driven into +Vsat. At this instant, the potential at point A is

$$V_A = \frac{R_2}{R_{1+}R_2}.(+Vsat)$$

This is called as upper threshold point or upper trigger point. When the input becomes more positive than UTP, the differential input is negative. Therefore, the output is driven in –Vsat. At this instant the potential at the point B

$$V_B = \frac{R_2}{R_{1+}R_2}.(-Vsat)$$

This is the lower threshold point. The output remains at –Vsat until input voltage becomes more negative than LTP.
When input crosses and becomes more negative than LTP, the differential input voltage is positive and the output becomes +Vsat.
V_{UTP} and V_{LTP} is calculated by

$$V_{UTP} = \frac{R_2}{R_{1+}R_2}.(+Vsat)$$

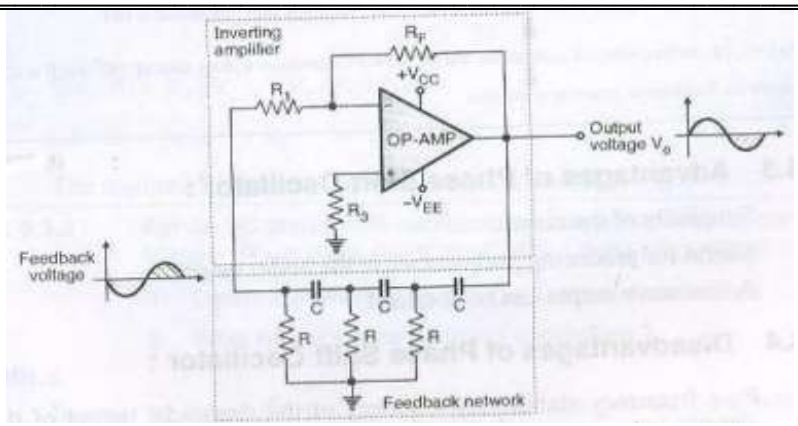
$$V_{LTP} = \frac{R_2}{R_{1+}R_2}.(-Vsat)$$

Explaination-2M

Waveform-1M

V_{UTP} and V_{LTP}-1M

	(c)	**Explain the circuit diagram of phase shift oscillator using op-amp.**	**6M**

	Ans:	 **Explanation:** The Op- Amp is used as an inverting amplifier. Therefore it introduces a phase shift of 180^0 between its input and output. The output of the inverting amplifier is applied at the input of the RC phase shift network. This network attenuates the signal at its input and feeds it to the amplifier input. The level of attenuation is decided by the feedback factor β. The gain of the inverting amplifier is decided by the values of RF and R1. This gain is adjusted in such a way that the product $\|A\beta\|$ is slightly greater than 1. It can be proved that the value of feedback factor β at the frequency of oscillations is β=1/29. For sustained oscillations, the loop gain $\|A\beta\| \geq 1$. Therefore, in order to make the loop gain $\|A\beta\| \geq 1$, the gain of the inverting amplifier A should be greater than or equal to 29. Gain of the inverting amplifier is given by, $\|A\| = RF / R1$ $Therefore, RF / R1 \geq 29$ or $RF \geq 29R1$ These values of RF and R1 will insure sustained oscillations. The expression for frequency of oscillations of an RC phase shift oscillator using OPAMP is given by $Fo= 1/ 2\pi\sqrt{RC}$	**Diagram-3M** **Explainatio n-3M**