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Subject Name: Microcontroller and applications Model Answer Subject Code:

22426

Important Instructions to examiners:

- 1) The answers should be examined by key words and not as word-to-word as given in themodel answer scheme.
- 2) The model answer and the answer written by candidate may vary but the examiner may tryto assess the understanding level of the candidate.
- 3) The language errors such as grammatical, spelling errors should not be given moreImportance (Not applicable for subject English and Communication Skills.
- 4) While assessing figures, examiner may give credit for principal components indicated in thefigure. The figures drawn by candidate and model answer may vary. The examiner may give credit for anyequivalent figure drawn.
- 5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
- 6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
- 7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q. N.	Answers	Marking Scheme
1	(A)	Attempt any FIVE of the following:	10- Total Marks
	(a)	State any four important features of 8051 microcontroller.	2M
	Ans:	 Features of 8051 microcontroller: (Any Four) 1) 8- bit data bus and 8- bit ALU. 2) 16- bit address bus - can access maximum 64KB of RAM and ROM. 3) On- chip RAM -128 bytes (Data Memory) 4) On- chip ROM - 4 KB (Program Memory) 5) Four 8-bit bi- directional input/output ports Four 8-bit bi- directional input/ output ports. 6) Programmable serial ports i.e. One UART (serial port) 7) Two 16- bit timers- Timer 0& Timer 1 8) Works on crystal frequency of 11.0592 MHz 9) Has power saving and idle mode in microcontroller when no operation is performed. 10) Six interrupts are available: Reset, Two interrupts Timers i.e. Timer 0 and Timer 1, two 	Each correct feature: ½ Mark

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	external hardware interrupts- INTO and INT1, Serial communication interrupt for both receive and transmit.								
(b)	Find out the number of address lines required to access 4 KB of RAM						2M		
Ans:	Ans: 12 address lines required to access 4 KB of RAM as $2^{12} = 4$ KB								Calculati on:1M
									Answer: 1M
(c)	List out a	ny two instru	ctions of follo	owing addr	essing mode	s:			2M
	(i) (ii)	Immediate Register ade	addressing. dressing.						
Ans:	(i)	Immediate a 1. MOV A, 2. MOV DP	addressing in: #36H TR, #27A2H	structions:					Each instructi on ½ M
	(ii)	Register add 1. MOV A, 2. MOV R7	Iressing. RO , A						
	(NOTE: Co	onsider any re	levant correc	t instructic	ons)				
(d)	Draw the	format of SC	ON register.						2M
Ans:									2M for
	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	Tormat
	SM0 SCO	ON.7 Seri	al port mode	specifier					Bitwise explaina
	SM1 SC	ON.6 Seri	al port mode	specifier					tion
	SM2 SC	ON.5 Use	d for multipr	ocessor cor	nmunication	(Make it 0	.)		optional
	REN SCO	ON.4 Set/	cleared by so	oftware to	enable/ disab	le receptio	on.		
	тва SCC	N.3 Not	widely used.						
	RB8 SCO	N.2 Not	widely used						
	ti sco	N.1 Tran mode	smit interrup 1. Must be	t flag. Set b cleared by	y hardware a software.	it the begir	nning of th	e stop Bit in	

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	$ \begin{array}{c} \hline \hline$	
g)	Define the term BUS related to microprocessor/controller and list different buses used in	2M
5,	microcontroller.	
Ans:	BUS: A Bus is a set of physical connections used for communication between CPU and peripherals.	Define:1
Ans:	BUS: A Bus is a set of physical connections used for communication between CPU and peripherals. Different buses used in microcontroller are:	Define: M List:1M
Ans:	BUS: A Bus is a set of physical connections used for communication between CPU and peripherals. Different buses used in microcontroller are: 1. Address Bus	Define:1 M List:1M
Ans:	BUS: A Bus is a set of physical connections used for communication between CPU and peripherals. Different buses used in microcontroller are: 1. Address Bus 2. Data Bus	Define: M List:1M

Q. No.	Sub Q. N.	Answers	Marking Scheme
2		Attempt any THREE of the following:	12- Total Marks
	a)	Draw the interfacing of stepper motor and write an ALP to rotate in anticlockwise direction	4M
	Ans:	Interfacing diagram of stepper motor with 8051:	Diagram :2M

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	H2: DJNZ R3, H2	
	DJNZ R2, H1	
	RET	
	(NOTE: Any other correct logic used for program should be considered)	
b)	Describe power down mode and ideal mode of 8051 with circuit diagram . which SFR is used to set these modes and draw the same.	4M
Ans:		
	IDLE MODE In the Idle mode, the internal clock signal is gated off to the CPU, but not to the Interrupt, Timer and Serial Port functions.	Power down
	The CPU status is preserved in its entirety, the Stack Pointer, Program Counter, Program	mode: M
	Status Word, Accumulator, and all other registers maintain their data during Idle. The port pins hold the logical state they had at the time idle mode was activated. ALE and PSEN hold at logic high levels. There are two ways to terminate the idle mode.	ldle Mode: M
	i) Activation of any enabled interrupt will cause PCON.O to be cleared and idle mode is terminated.	Identi ation o
	ii) Hard ware reset: that is signal at RST pin clears IDEAL bit IN PCON register directly. At this time, CPU resumes the program execution from where it left off.	PCON: M
	POWER DOWN MODE	PCON
	An instruction that sets PCON.1 causes that to be the last instruction executed before going into the Power Down mode. In the Power Down mode, the on-chip oscillator is stopped. With the clock frozen, all functions are stopped, but the on-chip RAM and Special Function Register are maintained held. The port pins output the values held by their respective SFRS. ALE and PSEN are held low. Termination from power down mode: an exit from this mode is hardware reset. Reset defines all SFRs but doesn't change on chip RAM	Forma 1M
	PCON (Power Control Register) SFR is used to set these modes.	



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	PCON: PC	WER	CONTR	OL RE	GISTE	r. not	BIT ADD	RESSA	BLE.		
	SMOD	_	_	_	GF1	GF0	PD	IDL]		
	SMOD Double by when the — Not imple — Not imple GF1 General p GF0 General p PD Power D	aud rate bi Serial Port emented, re emented, re purpose flag purpose flag own bit. S	t. If Timer is used in served for eserved for served for bit. bit. etting this	1 is used t modes 1, 2 future use. future use. future use. bit activate	o generate b 2, or 3. * *	oaud rate and own operatio	MOD = 1	, the baud n 51BH.	rate is double	3	
c)	IDL Idle Mod	e bit. Settin rnative f	g this bit a unction	tivates Idl s of por	e Mode ope t 3 of 80	ration in the	80C51BH. ontroller.				4M
Ans:					P3.0 P3.1 P3.2	RxD TxD ĪNT0					Each pin function :1/2 M
				-	P3.3 P3.4	INT1T0					
				Ĩ	P3.5 P3.6	$\frac{T1}{\overline{WR}}$					
				T							
	RXD it is use TXD it is use INTO used fo INT1 used fo T0 Timer 0 T1 Timer 1 WR external o RD external	ed for se ed for se or extern or external external data me data me	rial inpu rial outp nal interr al interr input input mory wr emory R	t port out port rupt 0 upt 1 ite strok ead stro	P3.7	RD					



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Q. No.	Sub Q. N.			Answers						Marking Scheme
3		Attempt any THREE of the following :							12- Total Marks	
	a) Draw the format of PSW register of 8051 microcontroller and explain the function of e bit.						tion of ea	ach	4M	
	Ans:	CYACCYPSW.7ACPSW.6F0PSW.5RS1PSW.4RS0PSW.3OVPSW.2PSW.1PPSW.01. CY: Carry flag.This flag is set whenesubtraction. It can alswhere "SETB C" stance2. AC: Auxiliary carryIf there is a carry fromThis flag is used by in:3. F0: Available to the4. RS0, RS1: RegisterThese two bits are usin given table. The usgets selected.1111	F0RS1Carry Flag.Auxiliary carry flag.Available to the userRegister bank selectRegister bank selectOverflow flag.User- definable bit.Parity flag. Set/clearindicate and Odd/ evver there is a carry ouo be set to 1 or 0 directds for "set bit carry" aflagn D3 and D4 during arstructions that perfore user for general putbank selects bitsed to select one of ther can use only one b101	RS0 for general p or bit 1. or bit 0. ed by hardwa ren number of at from the D octly by instru- nd "CLR C" for n ADD or SUB m BCD (bina r poses. e four registrank of registrank ank of registrank BED BE B B B B B B B B B B B B B B B B	OV ourpose. If 1 bit in t of 1 bit in t of 2 bit after uctions s or "clear 3 operati ry coded er banks er at one Space Sank 0 ((Bank 1 () Bank 3 ()	er an 8 bit uch as "SE carry". on, this bi decimal) from inter time. By in RAM 00H- 07H 08H-0FH 10H-17H 18H-1FH	p eycle to dator. addition TB C" t is set arithm rnal RA default f)	on or and CLR (; it is clea etic. M as sho t , bank 0	c″ ured.	2M format, 2M function

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	This flag is set whenever the result of a signed number operation is too large, causing the						
	high- order bit to overflow into the sign bit. In general, the carry flag is used to detect errors						
	in unsigned arithmetic operations. The overflow flag is only used to detect errors in signed						
	arithmetic operations.						
	6. P: Parity flag The parity flag reflects the number of 1s in the A (accumulator) register only. If the A register						
	contains an odd number of 1s, then P=1. P=0 if A has an even number of 1s.						
b)	Develop an ALP to generate square wave of 2 kHz on port pin P2.1 generate delay using 4I						
	timer 0 in mode 1. Assume crystal frequency of 11.0592 MHz.						
Ans:	Calculation:	1M-					
	Crystal frequency= 11.0592 MHz	Calculati					
	I/P clock = (11.059 X 10 ⁶)/12= 1000000 = 921.58KHz	on, 2M					
	Tin = 1.085μ sec	program					
	For 2 kHz square wave	, 1M					
	Fout = 2 KHz	commen					
	Tout = $1/2X 10^3$	ts					
	= 0.5 msec $= 500$ µ sec						
	So $T_{ON} = T_{OFF} = 250 \mu$ sec						
	$N = T_{ON} / Tin = 250/1.085 = 230.41$						
	$(65535 - 231 + 1 = (65305)_{10} = (FF19)_{16}$						
	Program:-						
	MOV TMOD. # 01H : Set timer 0 in Mode 1, i.e., 16 bit timer						
	12: MOV TLO # 19H : Load TL register with LSB of count						
	MOV THO # OFFH : load TH register with MSB of count						
	SETB TRO						
	11: INB TEO 11 : noll till timer roll over						
	CLR TRO						
	CPL P2 1 : complement port 2.1 line to get high or low						
	CLP TEO						
	CIMPL2 , clear timer had 0						
c)	State and explain the need of the following development tools microcontroller board:	4M					
	(i) Editor						
	(ii) Assembler						
	(iii) Compiler						
	(iv) Linker						
Ans:	1) Editor: An editor is a program which helps you to construct your assembly language	1M each					
	program in right format so that the assembler will translate it correctly to machine language.						
	So, you can type your program using editor. This form of your program is called as source						
	program and extension of program must be .asm or .src depending on which assembler is						

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	 used. The DOS based editor such as a type your program. 2) Assembler: An assembler is progracorrect binary/hex code for each inst Object file with extension .obj and liss syntax error in the program. 3) Compiler: Compiler is programs the binary/hex code for each command i file with extension .obj and list file with error in the program. 4) Linker: A linker is a program, which 	ams that translate assembly ruction i.e. machine code a st file with extension .lst ext nat translate C language pro .e. machine code and gene ith extension .lst extension. h combines, if requested, m	I language program to the nd generate the file called as rension. It is used to find ogram to the correct rate the file called as Object It is used to find syntax nore than one separately	s
	assembled object files into one execu generate .abs file and initializes it wit	utable program, such as two th special instructions to fac	o or more programs and also cilitate its subsequent	
d)	loading the execution. Some example LX 51 Enhanced Linker etc. List software and hardware interrup priorities.	es of linker are ASEM-51 BL	51, Keil u Vision Debugger, vector addresses and	4M
d) Ans:	loading the execution. Some example LX 51 Enhanced Linker etc. List software and hardware interrup priorities.	es of linker are ASEM-51 BL ots used in 8051 with their v Vector address	51, Keil u Vision Debugger, vector addresses and Interrupt priority	4M 2M-I
d) Ans:	loading the execution. Some example LX 51 Enhanced Linker etc. List software and hardware interrup priorities. Interrupt Source External Interrupt 0 –INT0	es of linker are ASEM-51 BL ots used in 8051 with their v Vector address 0003H	51, Keil u Vision Debugger, vector addresses and Interrupt priority 1	4M 2M-I 1M -
d) Ans:	loading the execution. Some example LX 51 Enhanced Linker etc. List software and hardware interrup priorities. Interrupt Source External Interrupt 0 –INT0 Timer 0 Interrupt	es of linker are ASEM-51 BL ots used in 8051 with their v Vector address 0003H 000BH	51, Keil u Vision Debugger, vector addresses and Interrupt priority 1 2	4M 2M-I 1M - Vect
d) Ans:	loading the execution. Some example LX 51 Enhanced Linker etc. List software and hardware interrup priorities. Interrupt Source External Interrupt 0 –INT0 Timer 0 Interrupt External Interrupt 1 –INT1	es of linker are ASEM-51 BL ots used in 8051 with their v Vector address 0003H 000BH 0013H	51, Keil u Vision Debugger, vector addresses and Interrupt priority 1 2 3	4M 2M-I 1M - Vect 1M- prior
d) Ans:	loading the execution. Some example LX 51 Enhanced Linker etc. List software and hardware interrup priorities. Interrupt Source External Interrupt 0 –INT0 Timer 0 Interrupt External Interrupt 1 –INT1 Timer 1 Interrupt	es of linker are ASEM-51 BL ots used in 8051 with their v Vector address 0003H 000BH 0013H 001BH	51, Keil u Vision Debugger, vector addresses and Interrupt priority 1 2 3 4	4M 2M-I 1M - Vect 1M- prior

Q. No.	Sub Q. N.	Answers	Marking Scheme
4		Attempt any THREE of the following :	12- Total Marks
	(a)	Develop an 8051 based system for traffic light controlling .Draw interfacing diagram and write ALP for the same.	4M

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LANE Direction	8051 LINES	TRAFFIC LIGHT
NORTH	P1.0(NR)	RED
and and and	P1.1(NY)	YELLOW
	P1.2(NG)	GREEN
SOUTH	P1.3(SR)	RED
	P1.4(SY)	YELLOW
	P1.5(SG)	GREEN
EAST	P1.6(ER)	RED
Contraction of the	P1.7(EY)	YELLOW
	P3.0(EG)	GREEN
WEST	P3.1(WR)	RED
	P3.2(WY)	YELLOW
	P3.3(WG)	GREEN

Process:

- 1. Allow traffic from W to E and E to W.
- 2. Yellow light ON.
- 3. Allow traffic from N to S and S to N
- 4. Yellow light ON.
- 5. Repeat Process

Program:

NR EQU P1.0

NY EQU P1.1

NG EQU P1.2

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	SR EQU P1.3		
	SY EQU P1.4		
	SG EQU P1.5		
	ER EQU P1.6		
	EY EQU P1.7		
	EG EQU P3.0		
	WR EQU P3.1		
	WY EQU P3.2		
	WG EQU P3.3		
	MOV P1,#00H		
	MOV P3,#00H		
	AGAIN: SETB NR	;North Red ON	
	SETB SR	; South Red ON	
	SETB EG	;East Green ON	
	SETB WG	; West Green ON	
	ACALL DELAY		
	CLR EG	;East Green OFF	
	CLR WG	;West Green OFF	
	SETB EY	; East Yellow ON	
	SETB WY	; West Yellow ON	
	ACALL Y_DELAY	; Small Delay for Yellow	

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	CLR EY	; East Yellow OFF	
	CLR WY	; West Yellow OFF	
	SETB ER	; East Red ON	
	SETB WR	;West Red ON	
	CLR SR	; South Red OFF	
	CLR NR	; North Red OFF	
	SETB NG	; North Green ON	
	SETB SG	; South Green ON	
	ACALL DELAY		
	CLR NG	; North Green OFF	
	CLR SG	; South Green OFF	
	SETB NY	; North Yellow ON	
	SETB SY	; South Yellow ON	
	ACALL Y_DELAY		
	CLR NY	; North Yellow OFF	
	CLR SY	; South Yellow OFF	
	CLR ER	; East Red OFF	
	CLR WR	; West Red OFF	
	AJMP AGAIN		
	DELAY: MOV R0,#	ŧOFFH	
	L:MOV R1,#0FFH		
	DJNZ R1,\$		
	DJNZ R0,L		
	RET		

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	Y_DELAY: MOV R2,#0FFH	
	DJNZ R2,\$	
	RET	
	END	
(b)	Compare Von-Neumana and Harvard Architecture (any four points)	4M
Ans [.]		1M

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	Sr.	Harvard Architecture	Van Neumann's Architecture	
	No			
	1.	Program Nemory	CPU Address 12-bits Address 12-bits Address 12-bits and Data Memory	
	2.	The Harvard architecture uses physically separate memories for their instructions and data.	The Van Neumann's architecture uses single memory for their instructions and data.	
	3.	Requires separate & dedicated buses for memories for instructions and data	Requires single bus for instructions and data.	
	4.	Its design is complicated	Its design is simpler.	
	5.	Instructions and data can be fetched simultaneously as there is separate buses for instructions and data which increasing operation bandwidth.	Instructions and data have to be fetched in sequential order limiting the operation bandwidth.	
(c)	List diff	erent timer modes of 8051 microcontro	oller and describe mode 2 with neat sketch	n. 4M
Ans:				1M- List,
	M1 0 0 1	M0 0 1 0	MODEDESCRIPTION013-bit timer116-bit timer28-bit auto-reload	1.5M- Diagram , 1.5M- describe
	1	1	3 Split mode	



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RET END

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MOV TH1,#-6 or MOV TH1,#0FAh	; 4800 baud rate	, 1M-
MOV SCON, #50H	; 8-bit data,1 stop bit, REN enabled	Comme
SETB TR1	; Start timer 1	nts
AGAIN: MOV A, #"M"	; transfer "M"	
ACALL MESSAGE		
MOV A, #"S"	; transfer "S"	
ACALL MESSAGE		
MOV A, #"B"	; transfer "B"	
ACALL MESSAGE		
MOV A, #"T"	; transfer "T"	
ACALL MESSAGE		
MOV A, #"E"	; transfer "E"	
ACALL MESSAGE		
SJMP AGAIN		
MESSAGE: MOV SBUF, A		
JNB TI, \$		
CLR TI		

0	Sub	Δηςωρης	Marking
No.	Q. N.	Answers	Scheme
5.		Attempt any TWO of the following:	12- Total Marks
	a)	Explain the various selection factors of microcontroller suitable for application.	6M
	Ans:		Any 6
		The selection of microcontroller depends upon the type of application. The following factors must be considered while selecting the microcontroller.	1 Mark— each
		1. Word length: The word length of microcontroller is either 8, 16 or 32 bit. As the	factor
		word length increases, the cost, power dissipation and speed of the microcontroller increases.	
		2. Power dissipation: It depends upon various factors like clock frequency, speed,	

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	low power microcontrollers		
	3. Clock frequency: The spee	ed of an embedded system depends upon the clock	
	frequency. The clock freque	ncy depends upon the application.	
	4. Instruction Set: On the bacategories 1. CISC 2. RISC.	sis of instructions microcontrollers are classified into two	
	CISC system improves softw	are flexibility. Hence it is used in general purpose systems.	
	RISC improves speed of the	system for the particular applications.	
	5. Internal resources: The in	ternal resources are ROM, RAM, EEPROM, FLASH	
	ROM, UART, TIMER, watch o	dog timer, PWM, ADC, DAC, network interface, wireless	
	interface etc. It depends up	on the application for which microcontroller is going to be used.	
	 6. I/O capabilities: The number of I/O ports, size and characteristics of each I/O port, speed of operation of the I/O port, serial port or parallel ports. These are the considerations needed to ascertain. 7.Memory: For mass production of microcontrollers ROM versions and for lesser production EPROM version or CPU version with external program memory is suitable 		
1			
b)	Develop a program to trans	fer block of 05 numbers. From memory location 50H to 60H.	6M
b) Ans:	Develop a program to trans	fer block of 05 numbers. From memory location 50H to 60H.	6M 4 M— Correct
b) Ans:	Develop a program to trans	e. Please check the logic and understanding of students	6M 4 M— Correct Program ,2 M-
b) Ans:	Develop a program to trans NOTE: Program may change ORG 0000H CLR PSW.3	 ifer block of 05 numbers. From memory location 50H to 60H. e. Please check the logic and understanding of students ; Program from 0000H ; select bank 0 	6M 4 M— Correct Program ,2 M- commen
b) Ans:	Develop a program to trans	e. Please check the logic and understanding of students ; Program from 0000H ; select bank 0 ;	6M 4 M— Correct Program ,2 M- commen ts
b) Ans:	Develop a program to trans NOTE: Program may change ORG 0000H CLR PSW.3 CLR PSW.4 MOV R3, #05H	 afer block of 05 numbers. From memory location 50H to 60H. be. Please check the logic and understanding of students ; Program from 0000H ; select bank 0 ; ; Initialize Byte counter 	6M 4 M— Correct Program ,2 M- commen ts
b) Ans:	Develop a program to trans NOTE: Program may change ORG 0000H CLR PSW.3 CLR PSW.4 MOV R3, #05H MOV R0, #50H	 afer block of 05 numbers. From memory location 50H to 60H. be. Please check the logic and understanding of students ; Program from 0000H ; select bank 0 ; ; Initialize Byte counter ; Initialize memory pointer for source array 	6M 4 M— Correct Program ,2 M- commen ts
b) Ans:	Develop a program to trans NOTE: Program may change ORG 0000H CLR PSW.3 CLR PSW.4 MOV R3, #05H MOV R0, #50H MOVR1,#60H	 afer block of 05 numbers. From memory location 50H to 60H. be. Please check the logic and understanding of students ; Program from 0000H ; select bank 0 ; ; Initialize Byte counter ; Initialize memory pointer for source array ; Initialize memory pointer for destination array 	6M 4 M— Correct Program ,2 M- commen ts
b) Ans:	Develop a program to trans NOTE: Program may change ORG 0000H CLR PSW.3 CLR PSW.4 MOV R3, #05H MOV R0, #50H MOVR1,#60H	 afer block of 05 numbers. From memory location 50H to 60H. be. Please check the logic and understanding of students ; Program from 0000H ; select bank 0 ; ; Initialize Byte counter ; Initialize memory pointer for source array ; Initialize memory pointer for destination array ; therefore R0 → Source pointer 	6M 4 M— Correct Program ,2 M- commen ts
b) Ans:	Develop a program to trans	 afer block of 05 numbers. From memory location 50H to 60H. be. Please check the logic and understanding of students ; Program from 0000H ; select bank 0 ; ; Initialize Byte counter ; Initialize memory pointer for source array ; Initialize memory pointer for destination array ; therefore R0 → Source pointer ; R1 → destination pointer 	6M 4 M— Correct Program ,2 M- commen ts

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	MOV @R1, A; Write number to destination arrayINC R0; Increment source memory pointer by 1INC R1; Increment destination memory pointer by 1DJNZ R3, UP; Decrement byte counter by 1; Is it zero? No, jump to UPHERE : SJMP HEREEND ; Stop	
c)	Sketch 8051 interfacing diagram to interface 4 LED's and 4 switches. Interface switches to port 0 and LED to port 1 upper nibble. Develop an ALP to read status of switches and operate LED's as per switch status.	6M
Ans:	Full to the second s	3 M - correct interfaci ng diagram, 3 M - correct program

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		PROGRAM TO DISPLAY STATUS OF SWITCHES ON LED:			
		ORG 0000H MOV P0, #0F0H ; Make P0 as input START: MOV A, P0 ; Read status of the key CINE A, #0F0H, CHECK1 ; Key pressed branch from Port 0 SJMP START ; Jump to start CHECK1: LCALL DELAY ; Call Key debounce delay MOV A, P0 ; Read data from port 0 CPL A ; Complement A MOV P1, A ; Send data to LED SJMP START ; Jump to start DELAY: MOV R1,#0FFH ; Delay program UP: MOV R2, #0FFH; HERE: DJNZ R2, HERE DJNZ R1, UP RET END			
0	Cub	A normana and a lateral and	Marking		
Q. No.	Q. N.	Answers S	Scheme		
6.		Attempt any TWO of the following : 1	12- Total		

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		Marks
a)	Develop an ALP to read temperature from LM 35 sensor. Draw the interfacing diagram with 8051	6M
Ans:	NOTE: Program may change. Please check the logic and understanding of students	3 M –
	The rest of the re	Correct
	1M25 Sensor	diagram,
	LM35 Sensor	3 M-
	+ 5V	Program
	123 VCC	Trogram
	P1.0 - P1.7	
	P2.0 ADD A IN1	
	P2.1 ADD B IN3 P2.2 ADD C IN4	
	P2.3 P2.4 P2.5 P2.5 P2.5 P2.5 P2.5 P2.5 P2.5 P2.5	
	P2.6 , EOC IN7 CLOCK CLOCK	
	8	
	5	
	1	
	Program:	
	ORG 0000H	
	ADDR_A BIT P2.0	
	ADDR_B BIT P2.1	
	ADDR_C BIT P2.2	
	SC BIT P2.3	
	ALE BIT P2.4	
	OE BIT P2.5	
	EOC BIT P2.6	

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MY_DATA EQU P1	
ORG 0000H	
MOV MY_DATA,#0FFH ; make P1 as input	
SETB EOC ; make EOC an input	
CLR ALE ; clear ALE	
CLR SC ; clear SC	
CLR OE ;clear OE	
CLR ADDR_C ; C=0	
CLR ADDR_B ; B=0	
CLR ADDR_A ; A=0(select channel 0)	
ACALL DELAY	
SETB ALE ;latch address	
ACALL DELAY	
BACK: SETB SC ;start conversion	
ACALL DELAY	
CLR ALE	
CLR SC	
HERE: JB EOC,HERE ; wait	
HERE1: JNB EOC,HERE1	
SETB OE	
ACALL DELAY	
MOV A, MY_DATA	
MOV P1, A	
CLR OE	
SJMP BACK	
DELAY : MOV R3,#25 ;Delay Subroutine	
L3: MOV R4,#100	
L2: MOV R5,#100	
L1: DJNZ R5,L1	
DJNZ R4,L2	
DJNZ R3,L3	
RET	
END	

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b)	Develop a program to toggle the L after receiving the external interr	ED's after every 500m sec connected to P1.0 and P1.1 upt on INT0.	6M
Ans:			4 M-
	NOTE: Program may change. Pleas	se check the logic and understanding of students	correct
	Solution :	5 5	progran
	Crystal freg=11.0592MHz		,1 IVI- delav
	Timer frequency=11.0592MHz	/12	calculat
	Time=12/11.0592MHz=1.085µ	S	on,1M-
	For delay of 50 ms,		comme
	50ms/1.085µs=46082		ts
	Therefore, count to be loaded	in TH1 and TL1 can be calculated as	
	65536 - 46082 =19454D=4BFE	н	
	Program:		
	Program: ORG 00 H		
	Program: ORG 00 H LJMP MAIN		
	Program: ORG 00 H LJMP MAIN ORG 0003 H		
	Program: ORG 00 H LJMP MAIN ORG 0003 H MOV TMOD, #10H	; Timer1, mode 1	
	Program: ORG 00 H LJMP MAIN ORG 0003 H MOV TMOD, #10H HERE : MOV R0, #0AH	; Timer1, mode 1 ; Counter for 500ms (50*10)delay	
	Program: ORG 00 H LJMP MAIN ORG 0003 H MOV TMOD, #10H HERE : MOV R0, #0AH BACK : MOV TL1, # B0H	; Timer1, mode 1 ; Counter for 500ms (50*10)delay ; load count value in TL1	
	Program: ORG 00 H LJMP MAIN ORG 0003 H MOV TMOD, #10H HERE : MOV R0, #0AH BACK : MOV TL1, # B0H MOV TH1, #3CH	; Timer1, mode 1 ; Counter for 500ms (50*10)delay ; load count value in TL1 ; load count value in TH1	
	Program: ORG 00 H LJMP MAIN ORG 0003 H MOV TMOD, #10H HERE : MOV RO, #0AH BACK : MOV TL1, # B0H MOV TH1, #3CH SETB TR1	; Timer1, mode 1 ; Counter for 500ms (50*10)delay ; load count value in TL1 ; load count value in TH1 ; start Timer 1	
	Program: ORG 00 H LJMP MAIN ORG 0003 H MOV TMOD, #10H HERE : MOV R0, #0AH BACK : MOV TL1, # B0H MOV TH1, #3CH SETB TR1 AGAIN : JNB TF1, AGAIN	; Timer1, mode 1 ; Counter for 500ms (50*10)delay ; load count value in TL1 ; load count value in TH1 ; start Timer 1 ; stay until timer rolls over	
	Program: ORG 00 H LJMP MAIN ORG 0003 H MOV TMOD, #10H HERE : MOV R0, #0AH BACK : MOV TL1, # B0H MOV TH1, #3CH SETB TR1 AGAIN : JNB TF1, AGAIN CLR TR1	; Timer1, mode 1 ; Counter for 500ms (50*10)delay ; load count value in TL1 ; load count value in TH1 ; start Timer 1 ; stay until timer rolls over ; stop timer	
	Program: ORG 00 H LJMP MAIN ORG 0003 H MOV TMOD, #10H HERE : MOV R0, #0AH BACK : MOV TL1, # B0H MOV TH1, #3CH SETB TR1 AGAIN : JNB TF1, AGAIN CLR TR1 CLR TF1	; Timer1, mode 1 ; Counter for 500ms (50*10)delay ; load count value in TL1 ; load count value in TH1 ; start Timer 1 ; stay until timer rolls over ; stop timer ; clear timer flag	
	Program: ORG 00 H LJMP MAIN ORG 0003 H MOV TMOD, #10H HERE : MOV R0, #0AH BACK : MOV TL1, # B0H MOV TH1, #3CH SETB TR1 AGAIN : JNB TF1, AGAIN CLR TR1 CLR TF1 DJNZ R0, BACK	; Timer1, mode 1 ; Counter for 500ms (50*10)delay ; load count value in TL1 ; load count value in TH1 ; start Timer 1 ; stay until timer rolls over ; stop timer ; clear timer flag ; if R0 is not equal to 0, reload timer	

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		CPL P1.1 RETI	; Toggle P1.1 ; repeat	
	MAIN :		; Enable the external interrupt 0	
			; P3.2 as input pin	
	HEKE :			
		LND		
c)	Explain the	following instruct	ions.	6M
	SWAP A			
	ADD C			
	MUL AB			
	CJNE A, add,	, radd		
	MOV A, R ₀			
	MOVX A, @ /	A + DPTR.		
An	s: SWAP A			1 M –
	Description:	This instruction ex	changes bits 0-3 of the Accumulator with bits 4-7 of the	each
	Accumulator	. This instruction is	identical to executing "RR A" or "RL A four times	on.
	Example:	MOV A, #59H	; A= 59H	
		SWAP A	; A= 95H	
	ADD C Description: carry. The res Example: AD accumulator.	This instruction is u sult is stored in acc DC A, R0 : Add con	used to perform addition of two eight-bit numbers along with cumulator which is the default destination. tents of accumulator, RO and carry .The result is stored in	
	MUL AB			
	Description: multiplication 8 bit ,lower b Example :MC MC	the multiplicand an n if the result is 8 k byte of result will b DV A,#10H DV B,#02 H	nd the multiplier must be in A and B registers. After bit it will be in the accumulator and if the result is larger than e in accumulator and higher byte will be in register B.	

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After execution A=20H,B=0 H

CJNE A, add, radd

Description: Compare the contents of the accumulator with the 8 bit data in memory address mentioned in the instruction and if they are not equal then jump to the relative address mentioned in the instruction.

Example: CJNE A, 04H, UP: Compare the contents of the accumulator with the contents of 04H memory and if they are not equal then jump to the line of instruction where UP label is mention

MOV A,R₀

Description: this instruction copies the contents of source register R0 into accumulator. The register R0 remains unaffected.

Example: Before Execution A=43 H, R0=32 H After execution A=32 H, R0-32H

MOVX A, @ A + DPTR. (Consider it as MOVC A,@A+DPTR)

Description: Copy the contents of code memory pointed by the sum of Accumulator and DPTR to the Accumulator

MOVC is a move instruction, which moves data from the code memory space. The address operand in this example is formed by adding the content of the DPTR register to the accumulator value. Here the DPTR value is referred to as the base address and the accumulator value is referred to as the index address.

(NOTE : If student has attempted to solve considering as above or attempted to solve as given in question paper, give appropriate marks)



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